

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
(1)	18/3/14	Introduction	1	BB		
(2)	19/3/14	Number base conversions Problem solving	1	BB		
(3)	20/3/14	Complement problem solving	1	BB		
(4)	21/3/14	Subtraction using 2's complement	1	BB		
(5)	21/3/14	Problem solving	1	BB		
(6)	24/3/14	Signed number arithmetic Problem solving	1	BB		
(7)	25/3/14	Problem solving	1	BB		
(8)	26/3/14	Binary codes 2's, 8, 4, 2, 1 Sec. & self-complement examples	1	BB		
(9)	27/3/14	BCD, BCD Addition Subtraction, 9's & 10's codes, Excess code	1	BB		
(10)	28/3/14	Excess addition, Sub Hamming code	1	BB		
(11)	1/4/14	2 var. Logic gates Boolean algebra	2	BB		
(12)	2/4/14	Encoding in minterms	2	BB		
(13)	3/4/14	Duality, Comp. universal gates	2	BB		
(14)	4/4/14	Parity check even & odd, SOP, POS problem solving	2	BB		
(15)	7/4/14	NAND NOR Realization, Register forms	2	B		

Register forms

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(16)	8/4/14	Problem Solving	2	BB		
(17)	9/4/14	problems on minimization	2	BB		
(18)	10/4/14	Inttr. K-map formation Examples	3	BB		
		2, 3, 4-map Examples				
(19)	11/4/14	4-v map examples Cof from pos from problem solving	3	B		
(20)	14/4/14	5-v map problem solving	3			
(21)	15/4/14	6-v map problem solving	3			
(22)	16/4/14	problem solving on all v-maps	3			
23	17/4/14	Tabular Method Examples	3			
24	18/4/14	Problem Solving on Tab. method	3			
25	21/4/14	Code Converter Examples, problem	3			
26	22/4/14	Full Comb. logic Examples, Half adder	4			
27	23/4/14	Full adder, half-full Subtractor	4			
28	24/4/14	4-bit parallel Adder, problem solving	4			
29	25/4/14	4-bit & 8-bit, 4-bit add/sub, BCD adder	4			
30	28/4/14	Excess adder, Carry ripple adder	4			
31	29/4/14	design Examples	4			
32	30/4/14	problem solving				
33	1/5/14	problem solving	4			

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34	2/5/14	Repetition	4	BB		
35	2/6/14	Design of decoder, gate level realization examples.	5	BB		
36	3/6/14	Comp ⁿ card design using decoder	5	BB		
37	4/6/14	Design of Demux Examples	5	BB		
38	5/6/14	f ⁿ . Realization, problem solving	5	BB		
39	6/6/14	problem solving	5	BB		
40	16/6/14	Higher order mux, demux	5	BB		
41	17/6/14	Examples, problem solving	5	BB		
42	18/6/14	Encoder design examples	5	BB		
43	19/6/14	Priority Encoder Examples, FA, HA using mux, decoder	5	BB		
44	20/6/14	Code converters using full adder	5	BB		
45	23/6/14	Introduct ⁿ to memory, Memory cell, RAM, ROM & PROM	6	BB		
46	24/6/14	Design of ROM Examples	6	BB		
47	30/6/14	Boolean f ⁿ . Realiz ⁿ using RAM ROM, problem solving	6	BB		
48	1/7/14	PLA, PAL concepts examples	6	BB		
49	8/7/14	Examples problem solving	6	BB		

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50	3/7/14	Design of PLA, PAL, programming tables, examples	6	BB		
51	4/7/14	Comparison, problemsolving	6	BB		
52	7/7/14	Int. Seq. Ckt classification, synch, asynchronous examples	7	BB		
53	8/7/14	Basic flip flops operation, truth tables	7	BB		
54	9/7/14	Excitation, char ⁿ tables, char ⁿ . Equation NAND, RS, latch flip flop	7	BB		
55	10/7/14	JK, T, D flip flop, T. Table excitation	7	BB		
56	11/7/14	Pre-set, clear concepts, conversion	7	BB		
57	14/7/14	Conversion & problemsolving	7	BB		
58	15/7/14	Design of ripple counter	7	BB		
59	16/7/14	Design of synchronous counters	7	BB		
60	17/7/14	John & King, counter examples, problemsolving	7	BB		
61	18/7/14	Problemsolving on counters	7	BB		

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62	21/7/14	Design of Register, buffer, decoder, counter, shift reg.	B 7	B B		
63	22/7/14	FSM concepts state assign. min. state reduction & display	8	B B		
64	23/7/14	Problem solving	8	B B		
65	24/7/14	Analysis of clocked SR, CR & D, JK & flip flops	8	B B		
66	25/7/14	Realization of CR & JK using flip flops	8	B B		
67	28/7/14	Concept of Mealy & Moore, problem solving				
68	29/7/14	Mealy to Moore & Moore Mealy conversion	8	B B		
69	30/7/14	Problem solving	8	B B		
70	1/8/14	Problem solving	8	B B		

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21/7/14